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明　細　書

発明の名称　欠陥検査方法および装置

特許請求の範囲

1．被検査物の欠陥を検査する方法であって、被検査物の表面全体を走査線で走査して信号を得、粗い欠陥位置を検出する第1の検査を行った後、前記粗い欠陥近傍を、前記第1の検査における走査線の走査間隔よりも細い走査間隔で走査線を走査して信号を得、精密な欠陥位置を検出する第2の検査を行うことにより、被検査物における精密な欠陥検査を行うことを特徴とする欠陥検査方法。

2．第1の検査によって、得られた信号が、精密検査時の走査速度との比に対応して当該信号の歪を補償するように変調されることを特徴とする特許請求の範囲第1項記載の欠陥検査方法。

3．被検査物の表面を走査線で走査して被検査物からの情報を検出し電気信号に変換するセンサと、このセンサからの電気信号に基づき被検査物における欠陥を検出する欠陥検出部とを備えている欠陥検査装置であって、前記走査線の走査速度を切り換える速度切換部と、第1の走査によって検出された被検出物における欠陥位置を記憶する記憶部と、前記速度切換部を低速に切り換え、前記記憶部に記憶された欠陥位置近傍において第2の検査を行わせる指令部とを備えていることを特徴とする欠陥検査装置。

4．センサが、二次元ホトセンサであることを特徴とする特許請求の範囲第3項記載の欠陥検査装置。

発明の詳細な説明

〔技術分野〕

本発明は、欠陥検査技術、特に、被検査物表面に走査線（例えば光等）を走査して信号を得、これに基づき欠陥を検出する技術に関し、たとえば、半導体装置の製造において、ウエハの外観上の欠陥を検出するのに使用して有効な技術に関する。

〔背景技術〕

半導体装置の製造において、ウエハの外観上の欠陥を検査する技術として、ウエハと一次元ホトセンサとを相対的に走査させて画像信号を得、こ

次に、前記欠陥検査装置の作用を説明して、本発明の一実施例である欠陥検査方法を説明する。

ここで、欠陥検出部２０は、ＣＣＤ１４からの現在の画像信号と所定時間前の遅延画像信号との差を採ることにより欠陥の位置、大きさを検出し、かつ、設計パターン発生部２２からの信号を重合することにより欠陥のウエハの層に対する位置を検出するように構成されているものとする。

本実施例においては、まず、指令部２６の指令により、第１切換スイッチ８は高速用電源９側に、第２切換スイッチ１９は変調部１７側に、第３切換スイッチ２１は変調器２３側にそれぞれ切り換えられる。ウエハ１を保持したＸＹテーブルのサーボモータ３，４はコントローラ７を介して高速用電源９から給電されてＸＹテーブル２をＸＹ方向に駆動する。これにより、ＣＣＤ１４はウエハ１に対して相対的に高速度で走査することになる。

今、ＣＣＤ１４のウエハ１に対する通常の走査速度（以下、低速度走査という。）下におけるＣＣＤ１４のシフト速度Ｓと、ＣＣＤ１４に対し直角方向（以下、Ｘ方向とする。）の走査速度ｘとの関係は、第２図に示されるような状況となるものとする。すなわち、ＣＣＤ１４のシフトが１回終了した時点において、絵素１４ａの幅Ｗだけ ＣＣＤ１４が進むように走査速度ｘは設定されているものとする。これにより、ＣＣＤ１４はウエハ１の全面を塗りつぶすように画像を採取することになる。そして、ウエハ１上に相対的に投影されたＣＣＤ１４の絵素１４ａの大きさを、たとえば、0.2μｍ×0.2μｍとした場合、検出すべき欠陥２７の最小の大きさを、たとえば、直径0.6μｍとすると、その欠陥２７の大きさは、第２図に斜線で塗りつぶしたようにしてＣＣＤ１４により検出されることになる。

ところが、ＣＣＤ１４のウエハ１に対する走査速度が、たとえば、低速度走査の２倍（ｘ×２）になった場合、第３図に示されるように、ＣＣＤ１４はそのシフトが１回終了した時点において２ピッチ進む状態となるため、ＣＣＤ１４による画像採取は走査Ｘ方向に伸びた状態になり、最小欠陥２７の検出は不可能になる。

そこで、本実施例においては、第２切換スイッチ１９の切り換えによってＣＣＤ１４と欠陥検出部２０との間に変調器１７を介挿することにより、高速走査による欠陥検出不能を克服するようにしている。すなわち、変調器１７はアナログ信号処理部１５、Ａ／Ｄ変換器１６を介して入力されて来るＣＣＤ１４からの画像信号を走査Ｘ方向に伸びた状態を補償できるように変調して欠陥検出部２０に送信する。補償するための変調の態様としては、たとえば、隣り合う絵素１４ａ、１４ａの画像信号成分を平均化させる、各絵素の画像信号を１つおきに採取する、各絵素の画像信号成分を２倍化させる等の方式が考えられる。

欠陥検出部２０は、変調器１７からの現在の信号と、所定時間前の遅延信号とを比較して差分信号をとることにより、欠陥を検出する。しかし、この欠陥検出信号は変調された信号に基づくため、欠陥２７の大きさを正確に表示しているものではなく、ウエハ１上における欠陥の位置のみを表示しているものとなる。

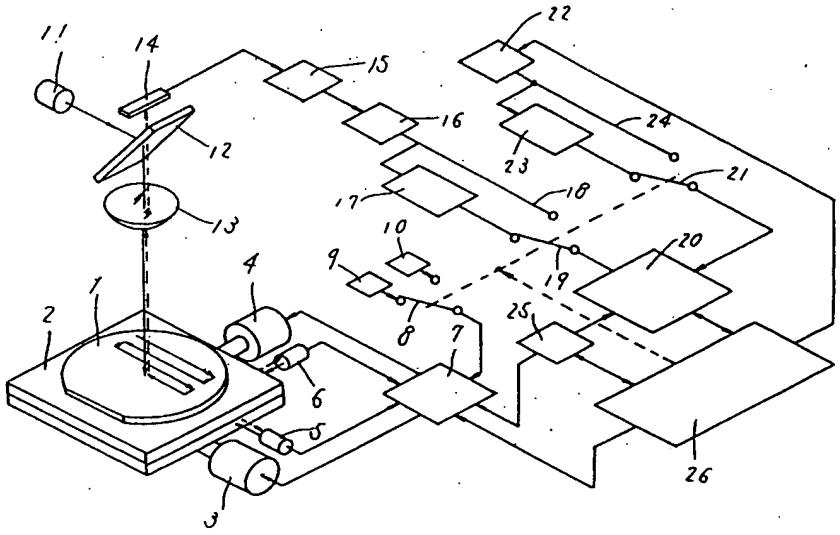
同時に、欠陥検出部２０には、設計パターン発生部２２からのパターン信号が第２変調器２３により第１変調器１７の変調に対応するように変調されて送信されており、この信号によって欠陥２７のウエハ１の層における位置が検出される。

欠陥検出部２０において検出された欠陥の各位置は、指令部２６に送信されてそのメモリー部に第４図に仮想的に示されるように記憶されて行く。

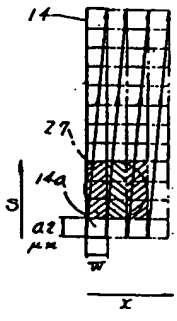
前記高速度走査による粗検査が終了すると、指令部２６はメモリー部に記憶された欠陥２７の位置を読み出す。続いて、指令部２６はＣＣＤ１４を、たとえば走査冒頭に最も近い欠陥２７の位置付近に高速度で相対的に移動させる。すなわち、指令部２６はコントローラ７に指令を送信してＸＹテーブル２を所望の方向に高速で移動させる。

ＣＣＤ１４が欠陥２７付近に達したことが測距器５，６等により確認されると、指令部２６は第１～第３切換スイッチ８，９，２１を低速側に切り換える。この切り換えにより、ＸＹテーブル２

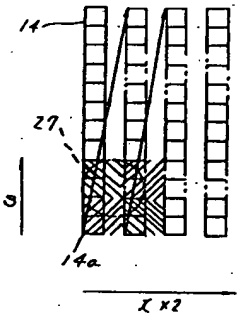
第　1　図



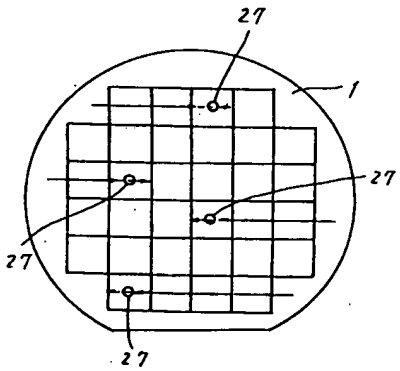
第　2　図



第　3　図



第　4　図



Translation of Ref. 3 (JP-A-60-245240)

Specification

The title of the invention: Method for the fault inspection and apparatus thereof

Claims

1. Method for detecting the faults in the object to be inspected, characterized by obtaining the first signals through the coarse inspection with the first (high speed) scan along the scanning lines on the whole surface of the object, obtaining then another signals through the another fine (low speed) scan along another scanning lines with smaller pitch than said first scan around only the locations indicated by said coarse inspection, whereby the pricise inspection for detecting the faults in the object to be inspected can be executed.

2. Method according to claim 1, characterized by modulating the signals obtained by the first inspection whereby the distortion of said siganals is compensated with the ratio of the high scanning speed for the fine inspection to the low scanning speed for the coarse inspection.

3. Apparatus for detecting the faults in the object to be inspectd, having sensors converting the informations obtained from the scan on the surface of the object to electric signals, a fault detector part detecting the faults in the object based on said electric signals which are supplied from said sensors, characterized by comprising scanning speed swithing part which can swith the scanning speed of said scanning lines, a memory part which can store the informations of the locations of the faults detected by the first high speed scan of the object , a command part

which make the sensor execute the second low speed scan around only the locations that had been stored in said memory part.

4. Apparatus according to claim 8, characterized by that said sensor is a two dimentional array of photosensors.

Detailed description of the invention

Technical field

This invention relates generaly to the technology for the inspection of the object such as semiconductor devices. In particulary, the invention relates to method and apparatus for detecting the faults in the object to be inspected, by using the signals obtained from the scan (for example, optical scan) of scanning lines on the object. The method and apparatus according to the invention proves fruitful as for curtailing the total inpection period for detecting externally appearing faults on the wafer in the manufacturing processes of semiconductor devices.

Background of art

As a possible technical method which inspects the externally appearing faults on the wafer, it is conceivable that the image signals are obtained by scanning the wafer relative to the one dimensional array of photosensors, whereby detect the faults on the wafer based on said image signals.

In such a method for the inspection of the faults, however, it has been pointed out by present inventors that there is a problem that long time are required for the inspection, since the speed of the scan in the course of the

inspection shoud be slow down to be able to detect even more small faults.

Moreover, in the recent tendancy that the size of the integrated circuits of semiconductor devices become small, intervals between the scanning lines shoud be required to be made much small.

As for a reference which describes the optical inspection apparatus for detecting the faults, see "Electronic Meterials (Denshi Zairyou)", extra volume, 1983, (Published by A Board of Industorial Investigation (Kohgyoh Chosakai), Nov. 18. 1982, p204-p209).

Objects of the invenstion

It is an object of the invention to provide a method for inspection of the faults by which the total inspection period can be curtailed.

The above and other objects and other novel features of the invanstion will become clear from the following description with reference to the figures in the attached drawings.

Summary of the invention

The present invention are summarized as follows.

As a first step according to the invention, firstly a coarse inspection for coarsely detecting the locations of the faults on the object to be inspected are executed by the high speed scan of sacanning lines on the whole surface of the object. Next, based on the result of this coarse inspection, it can be determined the limitted number of the locations that may have the faults and necessary to do fine inspection. Thereby, the total inspecrion period can be

curtailed by executing the fine inspection with low speed sacan around only the limitted number of the locations which were find out by said carse inspection.

Embodiments of the invention

Fig. 1 shows a block diagram of an embodiment of the fault inspection aparatus according to the invention. Fig. 2, 3 and 4 are diagrams explaining the processes of the fault inspection according to the invention.

In this embodiment, the fault inspection aparatus according to the invention comprises XY table 2 on which the wafer to be inspected is supported. The XY table 2 is driven by a pair of servomotor 3 and 4 through feed screws. The servomotors 3 and 4 are controlled by a controller 7 and the controller 7 is controlled in a manner of feedback based on the masured values obtained from the distance measuring device 5 and 6 which use laser. The first swich 8 is connected to the controller 7. The swich 8 can serve to connect the controller 7 to either a power supply 9 for high speed scan or a power supply 10 for low speed scan.

A light source 11 such as mercury lamp is arranged upward the XY table 2. The light source 11 can illuminate the wafer 1 on the table 2 through a half mirror 12 and a lens 13. One dimensional array of photosensors such as charge coupled device (CCD) 14 is arranged right above the wafer 1 through the half mirror 12 and the lens 13. By making the XY table 2 move relative to CCD 14, CCD 14 can scan the wafer in the X and Y directions.

CCD 14 is connected to a analog signal processor 15, and then the analog signal processor 15 is connected to a

operates such as that the fault inspection part 20 determines the locations and sizes of the faults from the differece signals between the current image signals and the delayed signals detected before a predetermined time interval and then by superimposing said differece signals on the signals from the design pattern generating part 22, the locations of the faults relative to the layer of the wafer can be detected.

In this embodiment, according to commands from the command part 26, the first switch 8 is switched to the side of the power supply 9 for high speed scanning, the second switch 19 is switched to the side of the modulation part 21, and the third switch 21 is switched to the side of the modulation part 23.

The wafer 1 is supported on the XY table and Servomotor 3, 4 are coupled to the XY table. By supplying electric power from the power supply 9 for high speed scanning through the cntroller7. The XY table is driven to the X and Y directions. In such msnner, CCD 14 may scan the whole surface of the wafer 1 with high speed.

Here, the relations between the shift speed S in the situation of the normal scan speed (which is called as the low scan speed in the followings) of CCD 14 relative to the wafer 1 and the scan speed x in the perpendicular direction (which is called as the x direction in the followings) may be supposed to be as shown in Fig. 2, that is, the scan speed x is supposed to be set as that when the shift of CCD 14 has completed one cycle, CCD 14 proceeds by the width W of the pixel 14a. As a result of the scanning operation in this

manner, CCD 14 can scan all pixels on the whole surface of the wafer 1. If the size of the image projected on the wafer 1 from pixels of CCD 14, is for example 0.2μm×0.2μm, and if minimum size of faults to be detected is for example the area of diameter 0.6μm, the minimum area of fault 27 to be able to detect by CCD 14 will be the shaded area shown in Fig. 2.

Hereupon, if the scanning speed of CCD 14 relative to the wafer 1 become for example two times of low scanning speed (x×2), when one cycle of the shift of the CCD 14 has been completed, the minimum image area scanned by the CCD 14 will be elongated toward the X direction, i.e., scanning direction. Therefore it will not be possible to detect the details of the minimum area 27 of the fault.

In the present embodiment, the problem that some faults can not be detected in the high speed scanning is then overcome by means of inserting the modulator part 17 through the second switch 19 between the CCD 14 and the fault detector part 20. That is, by means of that the image signals from CCD 14 are supplied to the fault detector part 20 through the modulator part 17 as well as the analog signal processor 15 and A/D converter 16, the image signals from CCD 14 are modulated so that the image signals elongated toward the x direction can be compensated. As possible modes of the modulation to carry out such a compensation, there will be for example averageing of the components of the image signals of the adjacent pixels, scanning alternately the components of the image signals of each pixels, doubling the components of the image signals,

switch to the sides of low speed scanning. By this switching, XY table 2 executes the predetermind low speed scanning. In this low speed scanning, CCD 14 executes normal scanning for the wafer 1, in which the pixels are scanned in a manner as shown in Fig. 2. Since the second swtch 19 has been switched to the path 18, the image signals obtained by this normal scanning are supplied to the fault detector part 20 through the path 18, not passing through the modulator 17. As for the faults 27 which are detected by the coarse inspection, the fault detector part 20 determine the normal locations, sizes and others of the faults based on the image signals. Since the third switch 21 is swtched to the path 24, the normal patten signals are then supplied from the design patten generator 22 to the fault detector part 20 through the path 24, whereby the locatins of the faults on the layer of the wafer 1 can be determined.

When the fine inspections around these locatins by the low speed scanning are completed, the command part 26 gives instructions to the wafer 1 that make CCD 14 relative to the wafer 1 move rapidly to the location of the next fault.

When CCD 14 reaches near the next fault, the command part 26 makes CCD 14 execute low speed scanning, whereby the fine inspection is executed as described above. Hereafter, fine inspections are executed for each of the locations of the faults obtained from the coarse inspection, and whereby the precise informations about the locations, sizes and so on of all faults on the whole surface of the wafer 1 can be obtained.

Effects of the invention

The invention described above has been shown for the case that the scope of the inventive cncept is applied to the inspection technology for the externally appearing faults. This case is the background of the field of use of the present invention. However, the scope of the present invention is not limitted to this application, but also can apply for example the inspection technology for the externally appearing faults of the mask or reticle, the inspection technology for the internal flaws and so on.

Brief description of the drawings

Fig. 1 is a block diagram of an embodiment.

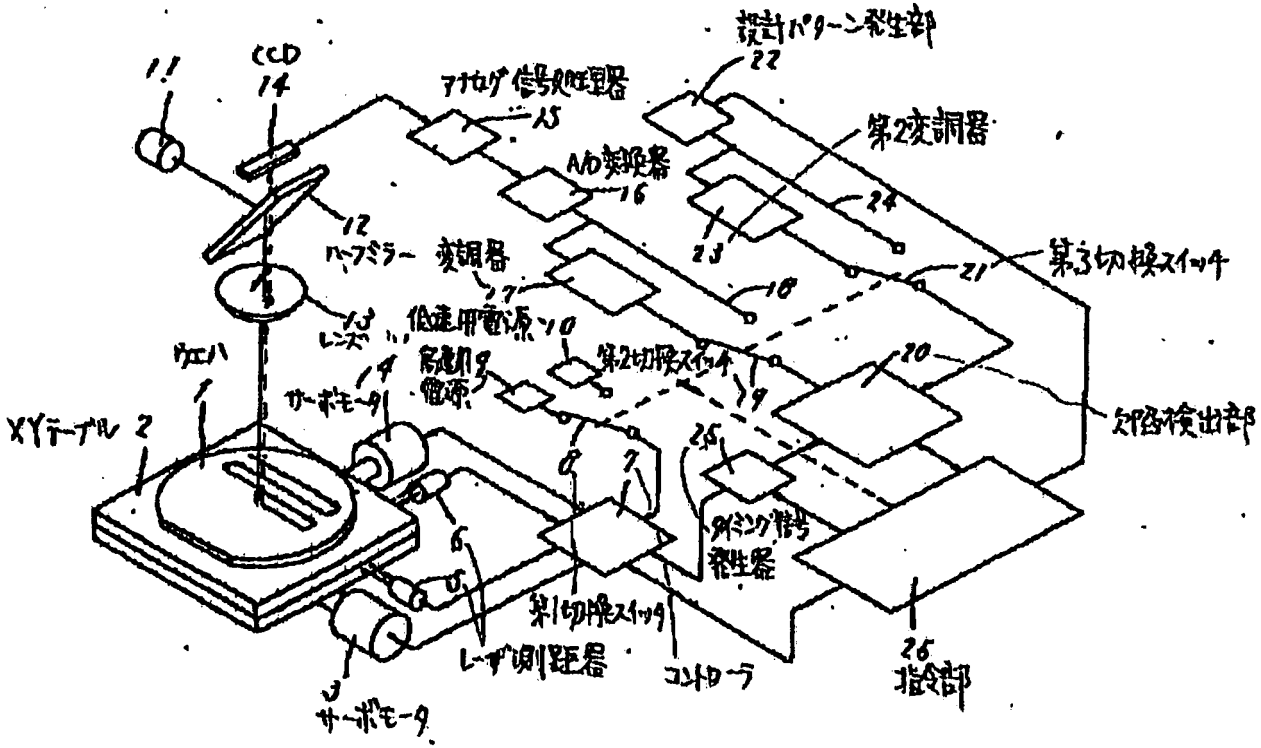
Fig. 2, 3 and 4 are diagrams illustrating details of the operation according to the invention.

Reference munbers of the components

1	wafer (object to be inspected)
2	XY table
3, 4	servomotor
5, 6	controller
7	distance measuring device
8, 19, 21	switch
9	power supply for high speed scanning
10	power supply for low speed scanning
11	light source
12	half mirror
13	lens
14	CCD (one dimensional array of photosensors)
15	analog signal processor
16	A/D converter
17, 23	modulator

18, 24	path
20	fault detector part
22	design pattern generator
25	timing signal generator
26	command part
27	fault

第　1　図



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